Customer No.: 31561
Application No.: 10/064,767
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REMARKS

Present Status of the Application

Applicants appreciate that the Office Action considers claims 4-5 and 14-15 to be allowable.

The Office Action rejects claims 1, 6-7, 8-11, and 16-18 under 35 U.S.C. 102 as being anticipated by Mesuda et al. (U. S. Patent 5,563,921; hereinafter Mesuda). The Office Action rejected claims 2-3 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mesuda in view of Pisipaty (U. S. Patent 6,628,112; hereinafter Pisipaty). Claims 1-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejects claims 1, 6-7, 8-11, and 16-18 under 35 U.S.C. 102 as being anticipated by Mesuda. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The present invention is directed to the signal jitter measuring device, which can be also implemented in a PLL, and the measuring method for the jitter. For example, independent claim 1 recites the features as follows:

> 1. A signal jitter measuring device for ***quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop***, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal therein, said measuring

device comprising:

a phase-relationship detection unit for ***outputting a phase relationship signal*** that corresponds to the phase relationship between ***said output signal and said input signal of the phase locked loop***; and

a jitter-level output unit coupled to said phase-relationship detection unit and responsive to ***said first phase difference signal, said second phase difference signal and said phase relationship signal for generating a jitter-level output signal that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop;***

wherein said jitter-level output signal is a pulse width difference between said first phase difference signal and said second phase difference signal. (*emphasis added*)

Independent claim 8 recited the similar features. Independent method claim 16, also recite the similar features as follows:

16. A method of measuring signal jitter which is capable of ***quantifying the jitters between an input signal and an output signal of a phase locked loop***, comprising the steps of:

providing a first phase difference signal and a second phase difference signal;

acquiring a phase relationship signal capable of showing whether the phase of said output signal leads or lags said input signal; and

acquiring a jitter value indicating the difference in pulse width between said first phase difference signal and said second phase difference signal according to said phase relationship signal. (*emphasis added*)

The present invention, as for example shown in FIG. 4, is to measure the jitter between the input signal S_in and the output signal S_out from the PLL. Wherein, the phase-relationship detection unit 405 can produce ***a phase relationship signal*** (jit-shrt) according to the signals S_in and S_out. The jitter-level output unit 402 is coupled to said phase-relationship detection

unit 405 and responsive to said first phase difference signal PDUP, said second phase difference signal PDDN and said phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out) that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop.

Further still, the two phase difference signals PDUP and PDDN are generated as recited in dependent claims 6-7, 9-10, and 17-18, which are described in FIGs. 5 and 6 as the example.

In re Mesuda, Fig. 1 (col. 7, lines 11-17; col. 8, lines 36-39; block 17, 18) fails to disclose the features discussed above. In Fig. 1 of Mesuda, the target signal having the frequency f1 and the reference signal having the frequency f3 are fed to the frequency converter. Clearly, the target signal having the frequency f1 might be the input signal S_in of the present invention, *but the reference signal having the frequency f3 is not the output signal S_out of the present invention.* The block 17 receives an output signal having the frequency |f1-f3| from the frequency converter (block 14) and an output signal having the frequency f2 from the voltage-controlled crystal oscillator (block 11), wherein f3=M * f2. Similarly, the output signal having the frequency f2 from the voltage-controlled crystal oscillator might be the output signal S_out of the present invention, *but the output signal having the frequency |f1-f3| from the frequency converter is not the input signal S_in of the present invention.* In summary, the jitter output signal of Mesuda's and the jitter-out signal of the present invention are generated based on different sources of signals.

Also and, the phase/frequency comparator 17 and the jitter detection filter 18 in the circuit of Fig. 1 fail to disclose the claimed phase-relationship detection unit 405 to produce ***a phase relationship signal*** (jit-shrt) according to the signals S_in and S_out.

The circuit in Fig. 1 also fail to disclose the features recited in claim 1 that the jitter-level output unit 402 is coupled to the phase-relationship detection unit 405 and responsive to the first phase difference signal PDUP, the second phase difference signal PDDN and the phase relationship signal (jit-shrt) for generating a jitter-level output signal (jitter-out).

Basically, Mesuda designs a different circuit in different operating mechanism.

With at least the same reasons, Mesuda fails to disclose the features recited in claim 8 and 16. Claims 1, 6-7, 8-11, and 16-18 are patently defining over Mesuda, and should be allowed.

With respect to claims 2-3 and 12-13, the Office Action further cites Pisipaty in combination. Pisipaty discloses a PLL circuit 400 in Fig. 4 (col. 5, lines 7-12). Data is fed to the D flip-flop 402 via the node 402, then a clock is output from the VCO 436. However, the PLL circuit 400 of Pisipaty does not provide the missing features in Mesuda to achieve the claimed invention. With at least the same forgoing reasons applied to claims 1 and 8, claims 2-3 and 12-13 patently define over Mesuda in view of Pisipaty.

For at least the foregoing reasons, Applicants respectfully submits that independent claims

1, 8, and 16 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-7, 9-15, and 17-18 patently define over the prior art references as well. Wherein, claims 4-5 and 14-15 are considered to be allowable.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-18 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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